IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Applicants:	Wing K Luk, et al.	Examiner:	Bernstein, Allison
Serial No.:	10/735,061	Group:	2824
Filed:	December 11, 2003	Docket:	YOR920030136US1 (8728-621)
For:	Gated Diode Memory Cells		

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313

APPEAL BRIEF

This Appeal is from a Final Office Action mailed on February 20, 2008. This Appeal was commenced by a Notice of Appeal and Pre-Appeal Brief Request for Review filed on May 20, 2008. A Notice of Panel Decision was mailed on January 2, 2009. Appellants hereby submit this Amended Appeal Brief in furtherance of the Appeal.

Appeal from Group 2824

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I. REAL PARTY IN INTEREST

The real party in interest for the above-identified application is International Business Machines Corporation, the assignee of the entire right, title and interest in and to the subject application by virtue of an assignment of recorded in the U.S. Patent and Trademark Office.

II. RELATED APPEALS AND INTERFERENCES

There are no Appeals or Interferences known to Applicant, Applicant's representatives or the Assignee, which would directly affect or be indirectly affected by or have a bearing on the Board's decision in the pending Appeal.

III. STATUS OF CLAIMS

Claims 1-33, 54, 55, and 58 are pending, of which Claims 11-33, 54, and 55 stand withdrawn. Claims 1-10 and 58 stand rejected and are under appeal. The claims are set forth in the attached Appendix.

IV. STATUS OF AMENDMENTS

No After Final Amendments have been filed.

V. SUMMARY OF CLAIMED SUBJECT MATTER

In general, the claimed inventions are directed to a gate diode memory cell. The gated diode memory cell includes a field effect transistor and gated diode, wherein a gate of the gated diode forms one terminal of a storage cell and a source of the gate diode forms another terminal. The gated diode memory cell may be used with an increased cell voltage during a Read operation for improving a sensing signal.

For purposes of illustration, the claimed inventions will be described with reference to certain Figures and corresponding text of Appellants' Specification, for example, but nothing herein shall be deemed as a limitation on the scope of the invention.

Claim 1 recites:

A gated diode memory cell comprising:

at least one transistor having a diffusion region and a gate terminal connected directly to a write wordline **(see, e.g., Spec. page 19, line 21 to page 20, line 6 with reference to FIG. 14 and FIG. 4 generally)**; and

a gated diode having a first terminal connected directly to the diffusion region of the at least one transistor and a second terminal connected directly to a read wordline **(see, e.g., Spec. page 14, lines 14-20 with reference to FIG. 4, and page 20, lines 4-7 with reference to FIG. 14)**.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

A. Rejections Under 35 U.S.C. § 102

i. Claims 1, 2 and 58 have been rejected under 35 USC 102(b) as being anticipated by Houghton et al. (USPN 5,757,693).

B. Rejections Under 35 U.S.C. § 103

i. Claims 3-10 are rejected under 35 U.S.C. § 103 as being unpatentable over Houghton in view of Hsu (US 2003/0147277).

VII. ARGUMENTS

A. Rejections Under 35 U.S.C. § 102

For a claim to be anticipated under 35 U.S.C. § 102, all elements of the claim must be found in a single prior art reference (see, e.g., *Scripps Clinic & Research Found. v. Genentech Inc.*, 927 F.2d 1565, 1576, 18 U.S.P.Q.2d. 1001, 1010 (Fed. Cir. 1991)). The identical invention must be shown in as complete detail as is contained in the claim. (See MPEP § 2131). The single prior art reference must disclose all of the elements of the claimed invention functioning essentially in the same manner (see, e.g., *Shanklin Corp. v. Springfield Photo Mount Corp*, 521 F.2d 609 (1st Cir. 1975)).

i. Claims 1, 2 and 58 have been rejected under 35 USC 102(b) as being anticipated by Houghton et al. (USPN 5,757,693).

Claim 1 claims, *inter alia*, "a gated diode having a first terminal connected directly to the diffusion region of the at least one transistor and a second terminal connected directly to a read wordline."

The teachings of Houghton are believed to be legally deficient to establish prima facie case of anticipation against the Claim 1 for at least the following reasons.

Houghton teaches a gain cell 20 comprising a write transistor Tw0, capacitor C0, storage node SN0, read transistor Tr0, and a diode D0 (see col. 2, lines 30-34 and FIG. 1).

As an initial matter, the rejection of Claim 1 in view of Houghton fails to address the limitation "connected directly to the diffusion region of the at least one transistor." Houghton specifically teaches that a storage node SN0 intervenes between the

transistor Tr0 and transistor Tw0 - which precludes the claimed structure of a direct connection. Thus, Houghton fails to teach "a gated diode having a first terminal connected directly to the diffusion region of the at least one transistor."

Further, Houghton does not teach "a gated diode having a first terminal connected directly to the diffusion region of the at least one transistor and a second terminal connected directly to a read wordline" as claimed in Claim 1. Houghton teaches that current is gated from BLR0 thru diode D0 and read transistor Tr0 (see FIG. 1 and col. 3, lines 10-11). The Examiner interprets the read transistor Tr0 to be a diode; respectfully, this interpretation has no support in the specification. For example, from FIG. 1, the structure of read transistor Tr0 is clearly that of a transistor; a transistor is a three terminal device. Indeed, Houghton is clear on the metes and bounds of the terms "diode" and "transistor", distinguishing between the two; consider for example that Houghton labels the diode as D0 and the read transistor as Tr0. It is clear from FIG. 1 of Houghton that the diode D0 is connected between a bitline and a transistor. Clearly, Houghton does not teach a diode including a terminal connected directly to a wordline.

Claim 1 is believed to be allowable over the teachings of Houghton for at least the foregoing reasons. Claims 2 and 58 depend from Claim 1. The dependent claims are believed to be allowable for at least the reasons given for Claim 1. Reversal of the rejection is respectfully requested.

B. **Rejections Under 35 U.S.C. § 103**

"In rejecting claims under 35 U.S.C. Section 103, the examiner bears the initial burden of presenting a *prima facie* case of obviousness." *In re Rijckaert*, 9 F.3d 1531, 1532, 28 USPQ2d 1955, 1956 (Fed. Cir. 1993) (citing *In re Oetiker*, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992)). It is well established that a *prima facie* showing of obviousness requires, in general, a two part analysis – starting with a claim interpretation analysis to determine the scope and substance of the subject matter being claimed, followed by an obvious analysis to determine whether the claimed subject matter (as interpreted) is obvious in view of the prior art. Once the claims have been properly constructed, the Examiner has the burden of establishing a *prima facie* case of obviousness. 'A *prima facie* case of obviousness is established when the teachings from the prior art itself would appear to have suggested the claimed subject matter to a person of ordinary skill in the art." *In re Bell*, 991 F.2d 781, 783, 26 USPQ2d 1529, 1531 (Fed. Cir. 1993) (quoting *In re Rinehart*, 531 F.2d 1048, 1051, 189 USPQ 143, 147 (CCPA 1976)).

i. Claims 3-10 are rejected as being unpatentable over Houghton in view of Hsu (US 2003/0147277).

Claims 3-10 depend from Claim 1. The dependent claims are believed to be allowable for at lease the reasons given for Claim 1. Reversal of the rejection is respectfully requested.

iii. Conclusion

Each of the 102 rejections in view of Houghton as applied to Claim 1 is believed to be legally defective for at least the reasons given above. The dependent claims, Claims 2-10 and 58, are believed to be allowable for at least the reasons given for Claim 1. Accordingly, withdrawal of the anticipation rejection is respectfully requested.

Respectfully submitted,

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VIII. Claims Appendix

1. (Rejected) A gated diode memory cell comprising:

at least one transistor having a diffusion region and a gate terminal connected directly to a write wordline; and

a gated diode having a first terminal connected directly to the diffusion region of the at least one transistor and a second terminal connected directly to a read wordline.

2. (Rejected) A gated diode memory cell as defined in Claim 1 wherein the first terminal of the gated diode forms one terminal of a storage cell and the second terminal of the gated diode forms another terminal of the storage cell.

3. (Rejected) A gated diode memory cell as defined in Claim 2 wherein the first terminal is a gate of the gated diode, wherein the gate is implemented in the form of a shallow trench.

4. (Rejected) A gated diode memory cell as defined in Claim 3, wherein the gate of the gated diode comprises a poly trench surrounded by thin oxide with silicon disposed underneath and surrounding the thin oxide.

5. (Rejected) A gated diode memory cell as defined in Claim 4 wherein the poly trench is cylindrical.

6. (Rejected) A gated diode memory cell as defined in Claim 4, wherein the gate of the gated diode comprises a metal oxide semiconductor ("MOS") capacitor.

7. (Rejected) A gated diode memory cell as defined in Claim 2 wherein the gate of the gated diode is planar.

8. (Rejected) A gated diode memory cell as defined in Claim 7 wherein the gate of the gated diode is disposed above a diffusion area.

9. (Rejected) A gated diode memory cell as defined in Claim 8, further comprising an oxide layer disposed between the gate of the gated diode and the diffusion area.

10. (Rejected) A gated diode memory cell as defined in Claim 7, wherein the gated diode comprises a planar metal oxide semiconductor ("MOS") capacitor.

11. (Withdrawn) A gated diode memory cell as defined in Claim 1 wherein:
the at least one transistor is a field effect transistor ("FET"); and
the first terminal of the gated diode is a gate in signal communication with the source of the FET.

12. (Withdrawn) A gated diode memory cell as defined in Claim 11, further comprising a metal connector in signal communication between the source of the field effect transistor and the gate of the gated diode.

13. (Withdrawn) A gated diode memory cell as defined in Claim 12 wherein the metal connector is a direct metal connector ("MCBAR").

14. (Withdrawn) A gated diode memory cell as defined in Claim 11 wherein:
the gate of the gated diode forms one terminal of a storage cell; and
the second terminal of the gated diode is a source of the gated diode that forms another terminal of the storage cell.

15. (Withdrawn) A gated diode memory cell as defined in Claim 14 wherein:
the drain of the FET is in signal communication with a bitline ("BL"); and
the gate of the FET is in signal communication with a write wordline ("WLw").

16. (Withdrawn) A gated diode memory cell as defined in Claim 15 wherein the source of the gated diode is in signal communication with a read wordline ("WLr").

17. (Withdrawn) A gated diode memory cell as defined in Claim 1 wherein:
the at least one transistor comprises first and second FETs with the source terminal of the first in signal communication with the gate terminal of the second; and
the first terminal of the gated diode is a gate of the gated diode in signal communication with the source terminal of the first FET.

18. (Withdrawn) A gated diode memory cell as defined in Claim 17 wherein:

the at least one transistor is a field effect transistor ("FET"); and

the gate of the gated diode is in signal communication with the source of the FET.

19. (Withdrawn) A gated diode memory cell as defined in Claim 18 wherein:

the gate of the gated diode forms one terminal of the storage cell; and

at least one of the source of the gated diode forms another terminal of the storage cell.

20. (Withdrawn) A gated diode memory cell as defined in Claim 19 wherein:

the drain of the FET is in signal communication with a bitline ("BL"); and

the gate of the FET is in signal communication with a write wordline ("WLw").

21. (Withdrawn) A gated diode memory cell as defined in Claim 20 wherein the bitline is a combined bitline in signal communication with a drain of an another FET in a single read/write configuration.

22. (Withdrawn) A gated diode memory cell as defined in Claim 20 wherein the bitline is a separated bitline in a dual read/write configuration.

23. (Withdrawn) A gated diode memory cell as defined in Claim 17 wherein:

The gate of the gated diode forms one terminal of the storage cell and at least one of the source of the gated diode forms another terminal of the storage cell.

24. (Withdrawn) A gated diode memory cell as defined in Claim 23 wherein:

the drain of the first FET is in signal communication with a bitline ("BL"); and

the gate of the first FET is in signal communication with a write wordline ("WLw").

25. (Withdrawn) A gated diode memory cell as defined in Claim 23 wherein at least one of the source of the gated diode is in signal communication with a read wordline ("WLr").

26. (Withdrawn) A gated diode memory cell as defined in Claim 1 wherein the gated diode comprises an implementing FET.

27. (Withdrawn) A gated diode memory cell as defined in Claim 26 wherein the drain of the implementing FET for the gated diode is left open.

28. (Withdrawn) A gated diode memory cell as defined in Claim 26 wherein the source of the implementing FET for the gated diode is left open, and the drain of the implementing FET for the gated diode becomes the source of the gated diode.

29. (Withdrawn) A gated diode memory cell as defined in Claim 26 wherein the drain of the implementing FET for the gated diode is connected to the source of the implementing FET for gated diode.

30. (Withdrawn) A gated diode memory cell as defined in Claim 1 wherein the gated diode comprises at least one "partial" FET.

31. (Withdrawn) A gated diode memory cell as defined in Claim 30 wherein the drain of the gated diode FET is left open to form one "partial" FET with the gate and source.

32. (Withdrawn) A gated diode memory cell as defined in Claim 30 wherein the source of the gated diode FET is left open to form one "partial" FET with the gate and drain, and the drain of the gate diode FET becomes the source of the gated diode.

33. (Withdrawn) A gated diode memory cell as defined in Claim 30 wherein the drain of the gated diode FET is connected to the source of the gated diode FET to form two "partial" FETs in parallel.

34~53. (Canceled)

54. (Withdrawn) A gate diode memory cell as defined in claim 1, wherein the gated diode is a two terminal active device which has a first capacitance when a voltage on the first terminal relative to the second terminal is in a first voltage range, and which has a second capacitance when the voltage on the first terminal relative to the second terminal is in a second voltage range, wherein said first and second voltage ranges are defined by a threshold voltage of the gated diode.

55. (Withdrawn) A gate diode memory cell as defined in claim 1, wherein the gated diode is a two terminal active device which has a first capacitance when a voltage on the first terminal relative to the second terminal is above a threshold voltage of the

gated diode, and which has a second capacitance, which is less than the first capacitance, when the voltage on the first terminal relative to the second terminal is below the threshold voltage.

56~ 57. (Canceled)

58. (Rejected) A gated diode memory cell as defined in Claim 1 wherein the at least one transistor and gated diode are a same type of FET (field effect transistor).

IX. Evidence Appendix

None.

X. Related Proceedings Appendix

None.